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Report on the Thesis "Hypercompression of Test Data" submitted by Sylvester Milewski

1. Problem and its impact

In his thesis Sylvester Milewski addresses the problem of test data explosion in microelectronics from two angles. While the first part of the thesis deals with the compaction of test sets generated by algorithms for automatic test pattern generation (ATPG), the second part introduces a new scheme for test data compression to minimize test data storage for in-system test. Although test compaction and test compression have been in the focus of research for many years, the growing complexity of integrated systems and the increasing volumes of high quality tests based on realistic defect analysis require advanced solutions. The topic of the thesis is therefore of utmost importance in the domain of electronic testing both from a research and from a practical perspective. The obtained results are discussed in more detail in the sequel.

2. Contribution

Sylvester Milewski presents his work in a well written manuscript consisting of seven chapters. In the introduction, he briefly introduces into the main concepts and challenges of testing digital logic. Starting from defect mechanisms and fault models, he explains the test generation problem and its complexity, sketches standard solutions for design for test (DFT), addresses the need for in-system test and discusses power-related issues during test. By showing the manifold reasons for test data explosion, he then motivates his work on test compaction and test compression and gives an overview of the envisaged solutions.

Chapter 2 summarizes the necessary background for the presented work. After giving a brief review of the state of the art in ATPG, Sylvester Milewski describes the basic principle of scan design and presents the "Embedded Deterministic Test" (EDT) scheme as an example for test compression. Finally, he introduces the *isometric compression* scheme in more detail, which provides the starting point for the new *hypercompression* scheme developed in this thesis. In isometric compression, potential toggles in a test cube are stored in a template register and the actual toggles are controlled by a hold register which is fed by an EDT decompressor. Characterizing a test pattern by its toggles, or alternatively by the run-length of zero or one sequences, is also used in many compression schemes relying on statistical coding. Therefore, I would have appreciated a more in-depth discussion of the strengths of isometric compression compared to these approaches.

Subsequently, the next two chapters are dedicated to Sylvester Milewski's contribution on test compaction. Before explaining the actual compaction strategy in Chapter 4, the underlying approach for computing necessary assignments is presented in Chapter 3. Here, Sylvester Milewski follows a simulation-based approach integrating advanced implication techniques known from the literature. Unfortunately, it is not always clear from manuscript where the presented approach goes beyond the state of the art or why other approaches from the literature, as for example working with 16-valued logic, are not considered. The algorithm for test compaction in Chapter 4 starts with fault classification after running a state-of-the-art ATPG tool with dynamic compaction. The main idea for compaction is then to identify faults which are only detected by a single pattern (or by a few patterns) and find groups of such faults with compatible necessary assignments. These fault groups are processed by a SAT-based ATPG algorithm which can target multiple faults at a time. Sylvester Milewski has implemented this idea by extending an existing SAT-based ATPG algorithm, such that the available necessary assignments can be added as additional constraints. The experimental analysis at the end of the chapter concentrates on the "tail" patterns produced by conventional ATPG, where the ratio of detected faults per pattern gets rather low. The results show that the proposed approach for test compaction can achieve reduction ratios between 4.58 % and 69.88 % for a set of industrial circuits. Although the differences can be explained by the structural properties of the circuits, a more detailed analysis would have been interesting for the reader, for example, by providing a more detailed statistic about numbers and sizes of successful fault groups.

In Chapter 5, Sylvester Milewski presents a new scheme for test data compression, which is based on the isometric compression scheme reviewed in Section 2.4. The new hypercompression architecture works with a much shorter template register. The complete information for a test cube is obtained by cycling through this register several times. Furthermore, the combination with an additional full toggle register allows for high toggle rates at dedicated scan chains. An associated synthesis flow provides algorithmic support for the new compression architecture. This comprises algorithms for template design as well as for the selection of toggle taps driving the phase shifter. To determine the structure of the template register, the degree of freedom for toggle points, which is introduced by the don't care bits in the test cubes, is properly exploited. Moreover, the synthesis flow benefits from a smart interleaving of ATPG and template design. The evaluation by a simulation study shows that the compression scheme compares favorably to standard EDT in terms of test pattern count, fill rate of test cubes, and switching activity. Nevertheless, for the reader it would have been very interesting and helpful to learn more details about the experimental study. This includes for example explicit compression ratios, a comparison to the isometric compression scheme, computation times, as well as the reasons for changing the set of example circuits.

Although the compression scheme of Chapter 5 already has a reduced power dissipation compared to standard EDT, Sylvester Milewski further improves the compression architecture and flow towards low power test in Chapter 6. The low-power architecture relies on a small set of even shorter templates, which can be set by sending the respective code together with the test pattern. The procedure for template generation extends the idea of necessary assignments by working with probabilities for assignments. In this context, necessary assignments are characterized by an assignment probability of one. The overall flow again interleaves ATPG and template generation in a smart way. The experimental analysis is based on a common subset of the example circuits used in the previous chapters. As intended, the power dissipation during scan operation can be reduced

considerably. Interestingly, the low-power compression scheme also shows a small reduction in test data volume.

Finally, Chapter 7 concludes the manuscript with a short short summary of the developed solutions and some future research directions.

Overall, Sylvester Milewski has developed very good solutions for a clearly formulated research problem of high relevance. In addition to the conceptual work, he has validated the proposed architectures and procedures by experimental case studies targeting large industrial designs. The achieved results are clearly ahead of the state of the art, which is also confirmed by his publications. In his list of references, two peer-reviewed papers directly related to the thesis can be found. One in an internationally recognized conference and another one in a high level IEEE journal. Moreover, due to the successful cooperation with Siemens Digital Industries Software, the thesis is also very strong with respect to its practical applicability. The underlying assumptions are based on realistic industrial data, and the developed procedures can easily be integrated into an industrial design flow.

The manuscript provides a clear description of the developed approaches and gives the expert reader a complete picture of the work. For the non-expert reader, it would have been helpful to include a more self-contained description of the state of the art. In particular, a more detailed introduction into standard techniques for test compaction and also into SAT-based ATPG would have provided a more self-contained description. Similarly, precise definitions of the used concepts and terminology would have strengthened the work. Furthermore, as already mentioned above, I would have appreciated a more detailed breakdown of experimental results, maybe in an appendix for interested readers. However, in my opinion, the excellent results achieved by Sylvester Milewski by far outweigh these issues in presentation.

3. Correctness

Sylvester Milewski's work is based on a thorough analysis of the state of the art, and his new contributions are supported by solid arguments. The experimental validation on a set of large industrial example circuits clearly shows that the developed techniques reach their goal.

4. Knowledge of the candidate

In his thesis Sylvester Milewski has demonstrated that he has comprehensive knowledge in the field of Information and Communication Technology, and in particular in the domain of electronic testing. The review of the state of the art in Chapter 2 covers all the relevant material and provides an excellent bibliography. Moreover, Sylvester Milewski's publication record by google scholar shows a remarkable list of publications and US patents, where more than half of these contributions are even outside the topic of the presented thesis. From my point of view this further emphasizes his excellent knowledge and research capabilities.

5. Conclusion

Taking into account what I have presented above and the requirements imposed by Article 13 of *the Act of 14 March 2003 of the Polish Parliament on the Academic Degrees and the Academic Title* (with amendments), my evaluation of the dissertation according to the three basic criteria is the following:

A. Does the dissertation present an original solution to a scientific problem? (the selected option is marked with **X**)

X				
Definitely YES	*Rather yes*	*Hard to say*	*Rather no*	*Definitely NO*

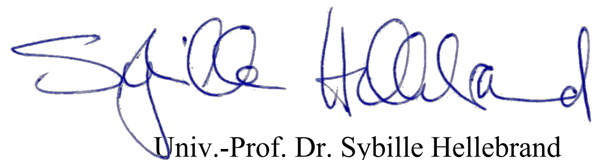
B. After reading the dissertation, would you agree that the candidate has general theoretical knowledge and understanding of the discipline of **Information and Communication Technology**, and particularly the area of **Electronic Testing**?

X				
Definitely YES	*Rather yes*	*Hard to say*	*Rather no*	*Definitely NO*

C. Does the dissertation support the claim that the candidate is able to conduct scientific work?

X				
Definitely YES	*Rather yes*	*Hard to say*	*Rather no*	*Definitely NO*

Overall, the thesis fulfills the requirements for the degree of Doctor of Philosophy as stated by the current law and its quality is clearly above the average. Therefore, I strongly recommend accepting thesis as submitted and rating it as “very good”.



Paderborn, January 5, 2022

Univ.-Prof. Dr. Sybille Hellebrand